ABSTRACT OF THE DISCLOSURE

A data transfer controller connects a high-speed bus to a low-speed bus. The controller includes an address register, a buffer, and a central controlling circuit. The address register stores an address allotted to a peripheral device connected to the low-speed bus. The stored address is referred to as preset address. The buffer stores a data retrieved from the peripheral device based on the preset address. The retrieved data is referred to as prefetched data. The central controlling circuit causes the prefetched data stored in the buffer to be outputted into the high-speed bus when a peripheral device address transmitted through the high-speed bus is identical to the preset address.

(Fig. 2)